REMARKS

The Applicants thank the Examiner for the careful examination of this application and respectfully request the entry of the amendments indicated hereinabove.

Claims 1-18 are pending and rejected. Claims 23-24 are new. Claims 1, and 7-11 are amended hereinabove.

The Applicants respectfully traverse the objection to the Specification on page 2 of the Office Action. The Applicants submit that the use of a resistor as the intervention circuit is clearly described in the Specification on page 11 line 11 (it is to be noted that 'intervention' is the same as 'keeper', as stated on page 5 line 7).

Claim 1 positively recites operating the intervention circuit to retain the row of memory cells in a desired state, and powering down, with a power switch, the circuitry for operating the row of memory cells preceding the intervention circuit. These advantageously claimed features are not taught or suggested by the patents granted to Itoh et al., Eto et al, or Yanagisawa et al.; either alone or in combination.

Eto et al. does not teach the advantageously claimed invention because Eto et al. does not teach powering down the circuitry for operating the row of memory cells preceding the intervention circuit. The Applicants submit that one or more of Eto et al.'s circuit terminals – including SWDZ shown in FIG. 5 – may be driven low or high as standard logic, but that is not considered a powering down step (column 5 lines 5-34).

In addition, Eto et al. teaches away from the advantageously claimed invention by teaching that the NMOS transistor (43) is only enabled in active mode (FIG. 7B). Furthermore, it is disabled in standby mode and/or when the pertinent memory block is unselected (FIG. 7A), which is the only situation where Eto et al. says that power is saved. Conversely, the Applicants NMOS transistor (114) is disabled in active mode and enabled in power down (e.g. power saving) mode.

Itoh et al. does not teach the advantageously claimed invention because Itoh et al. does not teach a powering down step (column 6 lines 15, 23, and 55-62, FIGS. 7a-8f). The Applicants submit that those with ordinary skill in the art know that bringing one of the inputs to a NAND gate low is not considered powering down. Moreover, there is a big difference between a power switch and a portion of the NAND gate.

Similarly, Yanagisawa et al. does not teach the advantageously claimed invention because Yanagisawa et al. does not teach a powering down step (page 8 paragraph 0111, FIG. 16B). The Applicants submit that those with ordinary skill in the art know that bringing one of the inputs to a NOR gate high is not considered powering down the NOR gate. Moreover, there is a big difference between a power switch and a portion of the NOR gate (FIG. 16B). The Applicants respectfully traverse the statement in the Office Action (Page 5) that signal a and the transistor connecting a and vdh precedes the intervention circuit. The Applicants submit that the identified transistor is part of the same NOR gate as the portion that is labeled the intervention circuit of Yanagisawa et al.; therefore it does not precede an intervention circuit.

Regarding Claim 3, the Applicants respectfully traverse the statement in the Office Action (page 3) that "...it would have been obvious to one with ordinary skill in the art to realize that transistors can be considered as resistors as well." The Applicants submit that transistors and resistors are not always interchangeable because transistors can be turned off and resistors cannot be turned off. The resistor only works in certain situations, such as the Applicants', where a high value resistor could be used to keep the wordline low in the sleep mode, yet have a weak enough pull down effect that the wordline could be raised by the wordline driver in the active mode.

Therefore, the Applicants respectfully traverse the Examiner's rejection of Claim 1 and respectfully assert that Claim 1 is patentable over the patents granted to Itoh et al., Eto et al, and Yanagisawa et al.; either alone or in combination. Furthermore, Claims 2-10 and 23 are allowable for depending on allowable independent Claim 1 and, in combination, including limitations not taught or described in the references of record.

Claim 11 positively recites an intervention circuit adapted to hold the row of memory cells at a desired state while control circuitry preceding the intervention circuit is powered down with a power switch. These advantageously claimed features are not taught or suggested by the patents granted to Itoh et al., Eto et al, or Yanagisawa et al.; either alone or in combination.

Eto et al. does not teach the advantageously claimed invention because Eto et al. does not teach powering down the control circuitry preceding the intervention circuit. The Applicants submit that one or more of Eto et al.'s circuit terminals – including SWDZ shown in FIG. 5 – may be driven low or high as standard logic, but that is not considered a powering down step (column 5 lines 5-34).

In addition, Eto et al. teaches away from the advantageously claimed invention by teaching that the NMOS transistor (43) is only enabled in active

mode (FIG. 7B). Furthermore, it is disabled in standby mode and/or when the pertinent memory block is unselected (FIG. 7A), which is the only situation where Eto et al. says that power is saved. Conversely, the Applicants NMOS transistor (114) is disabled in active mode and enabled in power down (e.g. power saving) mode.

Itoh et al. does not teach the advantageously claimed invention because Itoh et al. does not teach a powering down step (column 6 lines 15, 23, and 55-62, FIGS. 7a-8f). The Applicants submit that those with ordinary skill in the art know that bringing one of the inputs to a NAND gate low is not considered powering down. Moreover, there is a big difference between a power switch and a portion of the NAND gate.

Similarly, Yanagisawa et al. does not teach the advantageously claimed invention because Yanagisawa et al. does not teach a powering down step (page 8 paragraph 0111, FIG. 16B). The Applicants submit that those with ordinary skill in the art know that bringing one of the inputs to a NOR gate high is not considered powering down the NOR gate. Moreover, there is a big difference between a power switch and a portion of the NOR gate (FIG. 16B). The Applicants respectfully traverse the statement in the Office Action (Page 5) that signal a and the transistor connecting a and vdh precedes the intervention circuit. The Applicants submit that the identified transistor is part of the same NOR gate

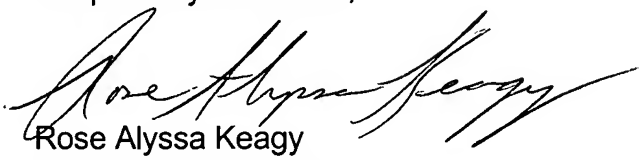
as the portion that is labeled the intervention circuit of Yanagisawa et al.; therefore it does not precede an intervention circuit.

Regarding Claim 3, the Applicants respectfully traverse the statement in the Office Action (page 3) that "...it would have been obvious to one with ordinary skill in the art to realize that transistors can be considered as resistors as well." The Applicants submit that transistors and resistors are not always interchangeable because transistors can be turned off but resistors cannot be turned off. The resistor only works in certain situations, such as the Applicants', where a high value resistor could be used to keep the wordline low in the sleep mode, yet have a weak enough pull down effect that the wordline could be raised by the wordline driver in the active mode.

Therefore, the Applicants respectfully traverse the Examiner's rejection of Claim 11 and respectfully assert that Claim 11 is patentable over the patents granted to Itoh et al., Eto et al, and Yanagisawa et al.; either alone or in combination. Furthermore, Claims 12-18 and 24 are allowable for depending on allowable independent Claim 11 and, in combination, including limitations not taught or described in the references of record.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,



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